Claims

The claims are not amended by this paper. This listing of claims is provided for the Examiner's convenience.

Listing of Claims

1. (Previously Presented) A semiconductor device comprising:

a semiconductor having at least channel, source and drain regions;

an insulating film formed on said semiconductor;

a gate electrode over the insulating film;

a first interlayer insulating film over said insulating film and the gate electrode;

a second interlayer insulating film on said first interlayer insulating film, said second interlayer insulating film comprising a different material from said insulating film;

a first opening in said insulating film for exposing a portion of said semiconductor;

a second opening in said first interlayer insulating film for exposing said portion of said semiconductor layer and a portion of said insulating film that surrounds said first opening; and

a third opening in said second interlayer insulating film for exposing said portion of said semiconductor, said portion of said insulating film and a portion of said first interlayer insulating film that surrounds said second opening,

wherein edges of at least said third opening are rounded off, and

wherein a thickness of the first interlayer insulating film is less than one third of a total thickness of the first and second interlayer insulating films.

2. (Previously Presented) A device according to claim 1 wherein a taper angle β of the second interlayer insulating film with respect to a major surface of said semiconductor in the third opening is larger than a taper angle α of the first interlayer insulating film with respect to the major surface of said semiconductor in the second opening.

3. (Previously Presented) A device according to claim 1, wherein said insulating film comprises silicon oxide.

4. (Previously Presented) A device according to claim 1, wherein said first and second interlayer insulating films comprise a material selected from the group consisting of silicon nitride and organic resin.

5. (Previously Presented) A device according to claim 1, wherein said second interlayer insulating film has a dry etching rate higher than said first interlayer insulating film.

6. (Previously Presented) A semiconductor device comprising:

a semiconductor layer formed over a substrate having an insulating surface, said semiconductor layer having at least channel, source and drain regions;

a gate insulating film over said semiconductor layer;

a gate electrode over the gate insulating film;

a first interlayer insulating film over said gate insulating layer and the gate electrode

a second interlayer insulating film on said first interlayer insulating film, said second interlayer insulating film comprising a different material from said gate insulating film;

a first opening in said gate insulating film for exposing a portion of said semiconductor layer;

a second opening in said first interlayer insulating film for exposing said portion of said semiconductor layer and a portion of said gate insulating film that surrounds said first opening; and

a third opening in said second interlayer insulating film for exposing said portion of said semiconductor layer, said portion of said gate insulating film and a portion of said first interlayer insulating film that surrounds said second opening,

wherein edges of at least said third opening are rounded off, and

wherein a taper angle β of the second interlayer insulating film with respect to a major surface of said semiconductor layer in the third opening is larger than a taper angle α of the first interlayer insulating film with respect to the major surface of said semiconductor layer in the second opening.

7. (Previously Presented) A device according to claim 6, wherein said gate insulating film comprises silicon oxide.

8. (Previously Presented) A device according to claim 6, wherein said first and second interlayer insulating film comprise a material selected from the group consisting of silicon nitride and organic resin.

9. (Previously Presented) A device according to claim 6, wherein said second interlayer insulating film has a dry etching rate higher than said first interlayer insulating film.

10. (Previously Presented) A semiconductor device comprising:

a semiconductor having at least channel, source and drain regions;

an insulating film on said semiconductor;

a gate electrode over the insulating film;

a first interlayer insulating film over said insulating film and the gate electrode;

a second interlayer insulating film on said first interlayer insulating film;

a first opening in said insulating film for exposing a portion of said semiconductor;

a second opening in said first interlayer insulating film for exposing said portion of said semiconductor and a portion of said insulating film that surrounds said first opening;

a third opening in said second interlayer insulating film for exposing said portion of said semiconductor, said portion of said insulating film and a portion of said first interlayer insulating film that surrounds said second opening; and

an electrode formed on said first, second, and third openings and connected with one of said source and drain regions through said first, second, and third openings,

wherein a taper angle β of the second interlayer insulating film with respect to a major surface of said semiconductor in the third opening is larger than a taper angle α of the first interlayer insulating film with respect to a major surface of said semiconductor in the second opening, and

wherein a thickness of the first interlayer insulating film is less than one third of a total thickness of the first and second interlayer insulating films.

11. (Previously Presented) A device according to claim 10, wherein said insulating film comprises silicon oxide.

12. (Previously Presented) A device according to claim 10, wherein said first and second interlayer insulating film comprise a material selected from the group consisting of silicon nitride and organic resin.

13. (Previously Presented) A device according to claim 10, wherein said second interlayer insulating film has a dry etching rate higher than said first interlayer insulating film.

14. (Previously Presented) A semiconductor device comprising:

a semiconductor layer formed over a substrate having an insulating surface and including at least channel, source and drain regions;

an insulating film on said semiconductor layer;

a gate electrode over the insulating film;

at least a first interlayer insulating film over the insulating film and over the gate electrode, and a second interlayer insulating film over the first interlayer insulating film;

at least one contact hole in said first and second interlayer insulating films and said insulating film, said contact hole having a tapered section; and

an electrode formed on said contact hole and connected with one of said source and drain regions through said contact hole,

wherein a taper angle β of an inner surface of the second interlayer insulating film in the contact hole with respect to a major surface of said semiconductor layer is larger than a taper angle α of an inner surface of the first interlayer insulating film in the contact hole with respect to said major surface of said semiconductor layer.

15. (Previously Presented) A device according to claim 14, wherein said insulating film comprises silicon oxide.

16. (Previously Presented) A device according to claim 14, wherein said first and second interlayer insulating film comprise a material selected from the group consisting of silicon nitride and organic resin.

17. (Previously Presented) A device according to claim 14, wherein said second interlayer insulating films has a dry etching rate higher than said first interlayer insulating layer.

18. (Previously Presented) A device according to claim 14, wherein angles of the tapered section of the contact hole decrease successively from the second interlayer insulating layer toward a first interlayer insulating layer.

19. (Previously Presented) A semiconductor device comprising:

a semiconductor having a channel region, at least one low doped impurity region, and at least one high doped impurity region said high doped impurity region being adjacent to said channel region with said low doped impurity region interposed therebetween;

an insulating film on said semiconductor;

a gate electrode over the insulating film;

at least a first interlayer insulating film over the insulating film and over the gate electrode, and a second interlayer insulating film over the first interlayer insulating film; and

a contact hole in said first and second interlayer insulating films and said insulating film for exposing a portion of said high doped impurity region, said contact hole including a first hole in the second interlayer insulating film, a second hole in the first interlayer insulating film, and a third hole in the insulating film, the contact hole having a tapered section such that the first hole has a larger cross section than the second hole, and the second hole has a larger cross section than the third hole,

wherein edges of said second interlayer insulating film in said contact hole are rounded off,

wherein angles of the tapered section of the contact hole decrease successively from the second interlayer insulating film toward the first interlayer insulating film, and

wherein a thickness of the first interlayer insulating film is less than one third of a total thickness of the first and second interlayer insulating films.

20. (Previously Presented) A device according to claim 19 wherein said insulating film comprises silicon oxide.

21. (Previously Presented) A device according to claim 19 wherein at least one of said first and second interlayer insulating films comprises a material selected from the group consisting of silicon nitride and organic resin.

22. (Previously Presented) A device according to claim 19 wherein said low doped impurity region includes phosphorus at a dose of 0.1 to 5 x 10^{14} atoms/cm^2.

23. (Previously Presented) A device according to claim 19 wherein said high doped impurity region includes phosphorus at a dose of 0.2 to 5 x 10^{15} atoms/cm^2.

24. (Previously Presented) A semiconductor device comprising:

a semiconductor layer formed over a substrate having an insulating surface and having a channel region, at least one low doped impurity region, and at least one high doped impurity region said high doped impurity region being adjacent to said channel region with said low doped impurity region interposed therebetween;

an insulating film on said semiconductor layer;

a gate electrode over the insulating film;

at least a first interlayer insulating film over the insulating film and over the gate electrode, and a second interlayer insulating film over the first interlayer insulating film;

a contact hole in said interlayer insulating films and said insulating film for exposing a portion of said high doped impurity region, said contact hole has a tapered section; and

an electrode formed on said contact hole and connected with one of said source and drain regions through said contact hole,

wherein edges of said interlayer insulating film in said contact hole are rounded off.

25. (Previously Presented) A device according to claim 24, wherein a taper angle β of an inner surface of the second interlayer insulating film in the contact hole with respect to a major surface of said semiconductor layer is larger than a taper angle α of an inner surface of first interlayer insulating film in the contact hole with respect to said major surface of said semiconductor layer.

26. (Previously Presented) A device according to claim 24, wherein angles of the taper shape of the contact hole decrease successively from the second interlayer insulating film toward the first interlayer insulating film.

27. (Previously Presented) A device according to claim 24 wherein said insulating film comprises silicon oxide.

28. (Previously Presented) A device according to claim 19 wherein at least one of said first and second interlayer insulating films comprises a material selected from the group consisting of silicon nitride and organic resin.

29. (Previously Presented) A device according to claim 24 wherein said low doped impurity region includes phosphorus at a dose of 0.1 to 5 x 10^{14} atoms/cm^2.

30. (Previously Presented) A device according to claim 24 wherein said high doped impurity region includes phosphorus at a dose of 0.2 to 5 x 10^{15} atoms/cm^2.

31. (Previously Presented) A device according to claim 1, wherein edges of said first opening are rounded off.

32. (Previously Presented) A device according to claim 1, further comprising an electrode connected with one of said source and drain regions through said first, second, and third openings.

33. (Previously Presented) A device according to claim 6, wherein edges of said first opening are rounded off.

34. (Previously Presented) A device according to claim 6, further comprising an electrode connected with one of said source and drain regions through said first, second, and third openings.

35. (Previously Presented) A device according to claim 19, wherein edges of said insulating film in said contact hole are rounded off.

36. (Previously Presented) A device according to claim 19, further comprising an electrode connected with one of said source and drain regions through said contact hole.

37. (Previously Presented) A device according to claim 24, wherein edges of said insulating film in said contact hole are rounded off.

38. (Previously Presented) A device according to claim 6, wherein a thickness of the first interlayer insulating film is less than one third of a total thickness of the first and second interlayer insulating films.

39. (Previously Presented) A device according to claim 14, wherein a thickness of the first interlayer insulating film is less than one third of a total thickness of the first and second interlayer insulating films.

40. (Previously Presented) A device according to claim 24, wherein a thickness of the first interlayer insulating film is less than one third of a total thickness of the first and second interlayer insulating films.

41. (Previously Presented) A device according to claim 14, wherein said first interlayer insulating film is formed on and in contact with the insulating film, and over the gate electrode, and said second interlayer insulating film is formed on and in contact with said first interlayer insulating film.

42. (Previously Presented) A device according to claim 19, wherein said first interlayer insulating film is formed on and in contact with the insulating film, and over the gate electrode, and said second interlayer insulating film is formed on and in contact with said first interlayer insulating film.

43. (Previously Presented) A device according to claim 24, wherein said first interlayer insulating film is formed on and in contact with the insulating film, and over the gate electrode, and said second interlayer insulating film is formed on and in contact with said first interlayer insulating film.

44. (Previously Presented) A semiconductor device comprising:

a metal layer formed over a glass substrate;

a first insulating film over the metal layer;

a second insulating film over the first insulating film;

a first opening in the first insulating film to expose a portion of the metal layer; and

a second opening in the second insulating film to expose a portion of the metal layer and a portion of the first insulating film,

wherein a first taper angle of the first insulating film in the first opening is smaller than a second taper angle of the second insulating film in the second opening.

45. (Previously Presented) The semiconductor device according to claim 44, wherein said first insulating film and said second insulating film are formed from a same material.

46. (Previously Presented) The semiconductor device according to claim 44, wherein at least any one of said first insulating film and said second insulating film are formed from silicon nitride.

47. (Previously Presented) A semiconductor device comprising:

a metal layer formed over a glass substrate;

a first insulating film over the metal layer;

a second insulating film over the first insulating film;

a first opening in the first insulating film to expose a portion of the metal layer; and

a second opening in the second insulating film to expose a portion of the metal layer and a portion of the first insulating film,

wherein a thickness of the first insulating film is less than one third of a total thickness of the first and second insulating films, and

wherein a first taper angle of the first insulating film in the first opening is smaller than a second taper angle of the second insulating film in the second opening.

48. (Previously Presented) The semiconductor device according to claim 47, wherein said first insulating film and said second insulating film are formed from a same material.

49. (Previously Presented) The semiconductor device according to claim 47, wherein at least any one of said first insulating film and said second insulating film are formed from silicon nitride.

50. (Previously Presented) A semiconductor device comprising:

a substrate having an insulating surface;

at least one thin film transistor formed over the substrate, the thin film transistor comprising a source region, a drain region, a channel formation region provided between the source region and the drain region, and a gate electrode provided adjacent to the channel formation region with a gate insulating film therebetween;

a multilayer insulating film provided over the thin film transistor and comprising at least two layers including a first insulating layer and a second insulating layer over the first insulating layer and comprising a different material from the first insulating layer;

a contact hole provided through the multilayer insulating film, the contact hole including a first opening through the first insulating layer and a second opening through the second insulating layer and concentric with the first opening; and

a wiring provided over the multilayer insulating film and electrically connected to one of the source region and the drain region through the contact hole,

wherein:

an edge of the second opening is rounded off;

a side surface of the multilayer insulating film in the contact hole is tapered such that the second opening exposes a portion of the first insulating film that surrounds the first opening; and

a thickness of the first insulating layer is less than one third of a total thickness of the multilayer insulating film.

51. (Previously Presented) A semiconductor device comprising:

a substrate having an insulating surface;

at least one thin film transistor formed over the substrate, the thin film transistor comprising a source region, a drain region, a channel formation region provided between the source region and the drain region, and a gate electrode provided adjacent to the channel formation region with a gate insulating film therebetween;

a multilayer insulating film provided over the thin film transistor and comprising at least two layers including a first insulating layer and a second insulating layer over the first insulating layer;

a contact hole provided through the multilayer insulating film, the contact hole including a first opening through the first insulating layer and a second opening through the second insulating layer and concentric with the first opening;

a pixel electrode provided over the multilayer insulating film and electrically connected to one of the source region and the drain region through the contact hole,

wherein:

an edge of the second opening is rounded off;

a side surface of the multilayer insulating film in the contact hole is tapered;

a thickness of the first insulating layer is less than one third of a total thickness of the multilayer insulating film; and

a side surface of the first insulating layer in the contact hole has a first taper angle and a side surface of the second insulating layer in the contact hole has a second taper angle, and the first taper angle and the second taper angle are different angles.

52. (Previously Presented) A semiconductor device comprising:

a substrate having an insulating surface;

at least one thin film transistor formed over the substrate, the thin film transistor comprising a source region, a drain region, a channel formation region provided between the source region and the drain region, and a gate electrode provided adjacent to the channel formation region with a gate insulating film therebetween;

a multilayer insulating film provided over the thin film transistor and comprising at least two layers including a first insulating layer and a second insulating layer over the first insulating layer;

a contact hole provided through the multilayer insulating film, the contact hole including a first opening through the first insulating layer and a second opening through the second insulating layer and concentric with the first opening;

a wiring provided over the multilayer insulating film and electrically connected to one of the source region and the drain region through the contact hole,

wherein:

an edge of the second opening is rounded off;

a diameter of contact hole is larger at a lowermost surface of the second insulating layer than at a lowermost surface of the first insulating layer;

a thickness of the first insulating layer is less than one third of a total thickness of the multilayer insulating film; and

a side surface of the first insulating layer in the contact hole has a first taper angle and a side surface of the second insulating layer in the contact hole has a second taper angle, and the first taper angle and the second taper angle are different angles.

53. (Previously Presented) A semiconductor device comprising:

a substrate;

an underlying insulating film formed over the substrate;

at least one thin film transistor formed over the substrate and the underlying insulating film, the thin film transistor comprising a source region, a drain region, a channel formation region provided between the source region and the drain region, and a gate electrode provided adjacent to the channel formation region with a gate insulating film therebetween;

a multilayer insulating film provided over the thin film transistor and comprising at least two layers including a first insulating layer and a second insulating layer over the first insulating layer;

a contact hole provided through the multilayer insulating film, the contact hole including a first opening through the first insulating layer and a second opening through the second insulating layer and concentric with the first opening;

a wiring provided over the multilayer insulating film and electrically connected to one of the source region and the drain region through the contact hole,

wherein:

an edge of the second opening is rounded off;

a side surface of the multilayer insulating film in the contact hole is tapered; and

a thickness of the first insulating layer is less than one third of a total thickness of the multilayer insulating film.

54. (Previously Presented) A semiconductor device comprising:

a substrate;

an underlying insulating film formed over the substrate;

at least one thin film transistor formed over the substrate and the underlying insulating film, the thin film transistor comprising a source region, a drain region, a channel formation region provided between the source region and the drain region, and a gate electrode provided adjacent to the channel formation region with a gate insulating film therebetween;

a multilayer insulating film provided over the thin film transistor and comprising at least two layers including a first insulating layer and a second insulating layer over the first insulating layer;

a contact hole provided through the multilayer insulating film, the contact hole including a first opening through the first insulating layer and a second opening through the second insulating layer and concentric with the first opening;

a pixel electrode provided over the multilayer insulating film and electrically connected to one of the source region and the drain region through the contact hole,

wherein:

an edge of the second opening is rounded off;

a diameter of contact hole is larger at a lowermost surface of the second insulating layer than at a lowermost surface of the first insulating layer;

a thickness of the first insulating layer is less than one third of a total thickness of the multilayer insulating film; and

a side surface of the first insulating layer in the contact hole has a first taper angle and a side surface of the second insulating layer in the contact hole has a second taper angle, and the first taper angle and the second taper angle are different angles.

55. (Previously Presented) The semiconductor device of claim 50, wherein the first insulating layer is made of silicon nitride.

56. (Previously Presented) The semiconductor device of claim 51, wherein the first insulating layer is made of silicon nitride.

57. (Previously Presented) The semiconductor device of claim 52, wherein the first insulating layer is made of silicon nitride.

58. (Previously Presented) The semiconductor device of claim 53, wherein the first insulating layer is made of silicon nitride.

59. (Previously Presented) The semiconductor device of claim 54, wherein the first insulating layer is made of silicon nitride.

60. (Previously Presented) The semiconductor device of claim 51, wherein the first taper angle is smaller than the second taper angle.

61. (Previously Presented) The semiconductor device of claim 52, wherein the first taper angle is smaller than the second taper angle.

62. (Previously Presented) The semiconductor device of claim 53, wherein the underlying insulating film comprises one of silicon oxide and silicon nitride.

63. (Previously Presented) The semiconductor device of claim 54, wherein the underlying insulating film comprises one of silicon oxide and silicon nitride.

64. (Previously Presented) The semiconductor device of claim 50, wherein the semiconductor device comprises an active matrix liquid crystal display.

65. (Previously Presented) The semiconductor device of claim 51, wherein the semiconductor device comprises an active matrix liquid crystal display.

66. (Previously Presented) The semiconductor device of claim 52, wherein the semiconductor device comprises an active matrix liquid crystal display.

67. (Previously Presented) The semiconductor device of claim 53, wherein the semiconductor device comprises an active matrix liquid crystal display.

68. (Previously Presented) The semiconductor device of claim 54, wherein the semiconductor device comprises an active matrix liquid crystal display.

69. (Previously Presented) A semiconductor display device comprising:

a semiconductor having at least channel, source and drain regions, with the source and drain regions being arranged on opposite sides of the channel region;

an insulating film over said semiconductor over the source and drain regions, the insulating film comprising a lower portion formed on the semiconductor and an upper portion over the lower portion; and

an opening in said insulating film for exposing a portion of said semiconductor, the opening including a first portion through the lower portion of the insulating film and a second portion through the upper portion of the insulating film;

wherein a first taper angle of the upper portion of the insulating film with respect to a major surface of said semiconductor in the second portion of the opening is larger than a second taper angle of the lower portion of the insulating film with respect to the major surface of said semiconductor in the first portion of the opening, and

wherein a thickness of the lower portion of the insulating film is less than one third of a total thickness of the insulating film.

70. (Previously Presented) The semiconductor display device of claim 69, wherein the insulating film comprise a material selected from the group consisting of silicon nitride and organic resin.

71. (Previously Presented) The semiconductor display device of claim 69, wherein:

the device comprises multiple openings in the insulating film for exposing portions of the semiconductor, each of the openings including a first portion through the lower portion of the insulating film and a second portion through the upper portion of the insulating film; and

for each opening, a first taper angle of the upper portion of the insulating film with respect to a major surface of the semiconductor in the second portion of the opening is larger than a second taper angle of the lower portion of the insulating film with respect to the major surface of the semiconductor in the first portion of the opening.

72. (Previously Presented) The semiconductor display device of claim 69, wherein one of the opening exposes the source region and another one of the openings exposes the drain region.

73. (Previously Presented) The semiconductor display device of claim 69, further comprising an electrode formed so as to connected with one of the source and drain regions through the opening.

74. (Previously Presented) The semiconductor display device of claim 69, wherein the insulating film comprises a first insulating film that defines the lower portion of the insulating film and a second insulating film that defines the upper portion of the insulating film.

75. (Previously Presented) The semiconductor display device of claim 74, further comprising a gate electrode formed between the first insulating film and the second insulating film.

76. (Previously Presented) The semiconductor display device of claim 69, wherein the opening exposes one of the source and drain regions.

77. (Previously Presented) A method for fabricating a semiconductor device, the method comprising:

forming a semiconductor film on an insulating surface;

forming an insulating film over the semiconductor film, the insulating film comprising a lower portion formed on the semiconductor film and an upper portion over the lower portion; and

forming an opening in the insulating film for exposing a portion of the semiconductor film, the opening including a first portion through the lower portion of the insulating film and a second portion through the upper portion of the insulating film;

wherein a first taper angle of the upper portion of the insulating film with respect to a major surface of said semiconductor film in the second portion of the opening is larger than a second taper angle of the lower portion of the insulating film with respect to the major surface of the semiconductor film in the first portion of the opening, and

wherein a thickness of the lower portion of the insulating film is less than one third of a total thickness of the insulating film.

78. (Previously Presented) The method for fabricating a semiconductor device according to claim 77, wherein:

forming the semiconductor film further comprises processing the semiconductor film to include at least channel, source and drain regions, with the source and drain regions being arranged on opposite sides of the channel region, and

forming the opening comprises forming the opening to expose the source or drain region.